C27 washing a surface of the gate insulating film with pure water in which ozone is dissolved;

B copy etching the surface of the gate insulating film with an acid solution which includes fluorine to remove at least one of B, Na, K, Mg, and Ca; and

a step of forming a gate conductive film in contact with said gate insulating film after said contaminant impurities are removed.—

REMARKS

The Official Action mailed January 17, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Month Extension of Time*, which extends the shortened period for response to May 17, 2002. Accordingly, Applicant respectfully submits that this response is being timely filed.

Claims 1-12 were pending in the present application. By this amendment, claims 1-4 have been amended and claims 13-15 have been added. Accordingly, claims 1-15 remain pending, of which claims 1-4 and 13-15 are independent.

Claims 1-12 stand rejected under 35 U.S.C. § 112, first paragraph as lacking enablement. As noted in MPEP § 2164.01:

> Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. The standard for determining whether the specification meets the enablement requirement was cast in the Supreme Court decision of *Mineral Separation v. Hyde,* 242 U.S. 261, 270 (1916) which postured the question: is the experimentation needed to practice the invention undue or unreasonable? That standard is still the one to be applied. *In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988). Accordingly, even though the statute does not use the term "undue experimentation," it has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. *In re Wands*, 858 F.2d at 737, 8 USPQ2d at 1404 (Fed. Cir. 1988).
> MPEP § 2164.01

The Applicants respectfully submit that the claims are enabled by the specification. The Examiner states that "there is no teaching as to the atmosphere in [the loader/unloader] chamber being different than clean room atmosphere prior to it's being placed under vacuum" (p.2, Paper No. 7). The Applicants respectfully disagree and direct the Examiner's attention to the disclosure in the specification at p. 3, lines 3-11, where the Applicants have described one embodiment of the invention where "since the step of washing the surface of the first film and a step of forming the second film are processed in sequence within one unit, the above steps are processed without exposure to the atmosphere including the interval between them." Further, Fig. 1 and the corresponding portion of the specification describe an apparatus where the above steps are performed without exposing the films to the atmosphere. In view thereof, it is respectfully submitted that a person skilled in the art can make and use the present invention without undue experimentation, and that the invention is therefore enabled.

Furthermore, the Examiner refers to a teaching at p. 9, lines 4-7 of the specification where the loader/unloader chamber 103 is vacuumed after the washing step and presumes that the loader/unloader chamber 103 is exposed to the atmosphere prior to vacuuming. However, the Examiner has not taken this step in context with the other processing steps which function to prevent the mixing in of contaminants from the atmosphere. For example, at p. 6, lines 8-13, the Applicants have disclosed purging washing chamber 110 with nitrogen gas to prevent the mixing in of contaminants from the atmosphere prior to vacuuming the loader/unloader chamber 103. For the reasons stated above, the Applicants request that the rejection under § 112 be reconsidered and withdrawn.

Claims 1-12 stand rejected under 35 U.S.C. § 112, second paragraph. In order to be definite, the claims must set out and circumscribe a particular subject matter with a reasonable degree of clarity and particularity. The Examiner argues that claims 1-12 are indefinite since "the atmosphere" lacks antecedent basis. The Applicants respectfully disagree. If the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992). The Applicants respectfully submit that one

with ordinary skill in the art would reasonably ascertain the meaning of the feature "wherein said ... steps are performed in sequence without being exposed to the atmosphere" and that "the atmosphere" refers to the ambient gaseous state found outside of the semiconductor manufacturing device described in the method claims of the present invention. For the reasons stated above, the Applicants request that the rejection under § 112 be reconsidered and withdrawn.

Claims 1-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Teramoto, U.S. Patent No. 5,773,325 (Teramoto) in view of Varhue, U.S. Patent No. 6,313,017 (Varhue) and Lampert et al., U.S. Patent No. 5,181,985 (Lampert). The Applicants respectfully traverse the Examiner's rejection because the Examiner has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the elements of amended independent claims 1-4. The present invention is generally directed to a method for manufacturing a semiconductor device, comprising the steps of

washing a surface of a film with pure water in which ozone is dissolved and etching the surface with an acid solution which includes fluorine to remove contaminant impurities such as B, Na, K, Mg, and Ca. Neither Teramoto, Varhue or Lampert, either alone or in combination, teach or disclose a method for manufacturing a semiconductor device, comprising the steps of washing a surface of a film with pure water in which ozone is dissolved and etching the surface with an acid solution which includes fluorine to remove contaminant impurities such as B, Na, K, Mg, and Ca.

For the reasons stated above, the Examiner has not set forth a *prima facie* case of obviousness; therefore, the Applicants respectfully request that the Examiner withdraw the § 103 rejection.

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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MARKED UP VERSION

1. (Amended) A method for manufacturing a semiconductor device comprising:

the first step of forming a semiconductor film;

the second step of etching the semiconductor film [removing] to remove contaminant impurities on a surface of said semiconductor film; and

the third step of forming a gate insulating film in contact with said semiconductor film after said second step;

wherein said second and third steps are performed in sequence without being exposed to the atmosphere.

2. (Amended) A method for manufacturing a semiconductor device comprising:

the first step of forming an amorphous semiconductor film;

the second step of forming a crystalline semiconductor film by crystallizing said amorphous semiconductor film;

the third step of forming an island-shaped crystalline semiconductor layer by patterning said crystalline semiconductor film;

the fourth step of etching the island-shaped crystalline semiconductor layer [removing] to remove contaminant impurities on a surface of said crystalline semiconductor layer; and

a fifth step of forming a gate insulating film in contact with said crystalline semiconductor layer after said fourth step,

wherein said fourth and fifth steps are performed in sequence without being exposed to the atmosphere.

3. (Amended) A method for manufacturing a semiconductor device comprising:

a first step of forming a base film;

a second step of etching the base film [removing] to remove contaminant impurities on a surface of said base film; and

the third step of forming a semiconductor film in contact with said base film after said second step,

wherein said second and third steps are performed in sequence without being exposed to the atmosphere.

4. (Amended) A method for manufacturing a semiconductor device comprising:

a step of forming a gate insulating film;

a step of etching the gate insulating film [removing] to remove contaminant impurities on a surface of said gate insulating film; and

a step of forming a gate conductive film in contact with said gate insulating film after said contaminant impurities are removed,

wherein said step of etching the gate insulating film to remove said contaminant impurities and said step of forming said gate conductive film are performed in sequence without being exposed to the atmosphere.

Please add new claims 13-15.

13. (New) A method for manufacturing a semiconductor device comprising:

forming a semiconductor film;

washing a surface of the semiconductor film with pure water in which ozone is dissolved;

etching the surface of the semiconductor film with an acid solution which includes fluorine to remove at least one of B, Na, K, Mg, and Ca; and

forming a gate insulating film in contact with said semiconductor film.

14. (New) A method for manufacturing a semiconductor device comprising:

forming a base film;

washing a surface of the base film with pure water in which ozone is dissolved;

etching the surface of the base film with an acid solution which includes fluorine to remove at least one of B, Na, K, Mg, and Ca; and

forming a semiconductor film in contact with said base film.

15. (New) A method for manufacturing a semiconductor device comprising:

forming a gate insulating film;

washing a surface of the gate insulating film with pure water in which ozone is dissolved;

etching the surface of the gate insulating film with an acid solution which includes fluorine to remove at least one of B, Na, K, Mg, and Ca; and

a step of forming a gate conductive film in contact with said gate insulating film after said contaminant impurities are removed.